UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,454	06/14/2006	Gunnar Nitsche	DE030429	6868

65913 7590 06/30/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
GOODLEY, JAMES E	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
06/30/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/596,454	NITSCHE ET AL.	
	Examiner	Art Unit	
	JAMES E. GOODLEY	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9 and 10* is/are rejected.

7)☒ Claim(s) *6-8 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 9 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 9 refers to a second phase detector, but no such disclosure is made in the application.

It appears there was mere oversight in claim drafting and that claim 9 should read, "...wherein the output of the voltage-controlled frequency generator is connected to a second phase detector input..."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Tarusawa et al. (European Patent Application Publication 360,442)***.

Regarding **claims 1-4**, Fig. 8 of Tarusawa discloses a method for interference compensation in a phase-locked loop comprising a voltage-controlled frequency generator [phase locked loop components], wherein the frequency generator is tuned to a nominal frequency via a tuning voltage [Vs] and whose actual frequency is compared with a reference frequency [reference signal] by means of a frequency comparison [1] and is tuned if a deviation is discovered via the frequency comparison, in which method in the event of interference [switching frequency setting to divider 2] the tuning voltage is changed by an interference voltage Vstor [shift in tuning voltage caused by the change in frequency setting of the divider] that depends on the interference event and thus a frequency deviating from the nominal frequency is generated, which is corrected again by the phase-locked loop, characterized in that if a known interference event occurs, a voltage Vcomp [Vda] which compensates for the interference voltage Vstor is generated in synchronism with this with sign inversion and is superimposed on the interference voltage (the compensation voltage Vda will alter the tuning voltage Vs, sent to the VCO).

Vcomp is determined in a measuring operation for all the possible known interference events (all possible settings of N in divider 2), and that this is stored in a compensation table (see ROM table in control circuit 7 of Fig. 15).

The measuring operation and the storage of the voltage values in the compensation table take place when the arrangement is made operative (when the frequency settings and compensation voltages are calibrated and stored).

The relevant compensation voltage value which is saved in the compensation table is read out prior to a known interference event (when data is entered to the control circuit, but before the divider value is switched to cause the interference event), which event causes interference voltage Vstor to occur, and with this compensation voltage value the compensation voltage Vcomp is controlled in synchronism with the occurrence of the interference voltage.

Regarding **claim 5**, Fig. 8 of Tarusawa discloses an arrangement for interference compensation in a phase-locked loop comprising a voltage-controlled frequency generator [elements of the phase locked loop], wherein the frequency generator has a Vtune input [Vs] and a VarGND terminal [direct connection between capacitor 19 and DAC 6], characterized in that the VarGND terminal for the voltage-controlled frequency generator is connected to a controllable voltage source [DAC 6, which produces a compensating voltage Vda, according to a change in frequency setting].

Allowable Subject Matter

Claims 6-8 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9 and 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding **claims 6 and 7**, the prior art of record fails to disclose or fairly suggest wherein the controllable voltage source comprises a resistor connected between the VarGND terminal and the GND potential and a controllable current source connected between the VarGND terminal and the resistor.

Regarding **claim 8**, the prior art of record fails to disclose or fairly suggest wherein the VarGND terminal is connected to the controllable voltage source via a voltage divider in such a way that the voltage divider is connected via a first partial resistor to the controllable voltage source, and the second partial resistor, which is connected in series, is connected to the GND potential and the VarGND terminal with the connection to the first partial resistor is connected to the second partial resistor.

Regarding **claims 9 and 10**, the prior art of record fails to disclose or fairly suggest wherein a phase detector charge pump (1) is arranged to which a reference clock is applied via a first phase detector input (PDin1), wherein the output of the phase detector charge pump (Cpout) is connected to the input of a voltage-controlled frequency generator (3) via a loop filter (2), wherein the output of the voltage-controlled frequency generator (3) is connected to a second phase detector (PDin2) via a frequency divider (4), wherein, furthermore, a measuring circuit is arranged, and wherein the loop filter (2) comprises a first capacitor at the input end, a third capacitor at the output end, a second resistor arranged between the input and the output of the loop filter and a series circuit which is connected to the input and comprises a first resistor

and a second capacitor, wherein the second capacitor of the series circuit is connected to the input of the measuring circuit, while the input in the measuring circuit forms a virtual ground terminal.

Regarding **claim 11**, the prior art of record fails to disclose or fairly suggest wherein a measuring circuit is connected to the Vtune input of the voltage-controlled frequency generator (3), that the measuring circuit comprises a first operational amplifier which works as a buffer amplifier whose output is connected via a first resistor and a capacitor to the inverting input of a second operational amplifier, working as a negative-feedback inverting amplifier, that the non-inverting input of the second operational amplifier is connected to a reference voltage, that the output of the second operational amplifier is fed back to the inverting input via two anti-parallel diodes, that the output of the second operational amplifier is further connected via a second resistor to the connection of the first resistor and the capacitor, and the output of the second operational amplifier has a TDet terminal for outputting a voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES E. GOODLEY whose telephone number is (571)272-8598. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/James E Goodley/

Examiner, Art Unit 2817

/Robert Pascal/

Supervisory Patent Examiner, Art Unit 2817